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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/691,274
Filing Date: October 22, 2003
Appellant(s): WERNER ET AL.

Scott F. Diring
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 29, 2008 appealing from the Office action mailed August 20, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,348,736	McGahay et al.	02-2002
5,610,105	Vines et al.	03-1997
2002/0090822	Jiang et al.	07-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 11-15, and 23-24, are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent No. 6,348,736 (McGahay et al., hereinafter referred to as McGahay) in view of U. S. Patent No. 5,610,105 (Vines et al., hereinafter referred to as Vines).

McGahay, in the abstract, in col 3, lines 63-67, in col 4, lines 1-46, discloses forming a low-k dielectric layer (SSQ, is a silicon-based dielectric layer) on a substrate, positioning the SSQ coated substrate in a plasma chamber and converting by plasma

oxidation an upper portion of the SSQ layer to a silicon dioxide layer so as to form a thin oxide layer (cap layer), and patterning the thin oxide layer (sacrificial layer) and the low-k dielectric layer (SSQ layer), wherein the thickness of the thin oxide layer formed is designed so as to cause minimal damage to the underlying SSQ layer, and minimal increase in capacitance in the final structure (i.e., the cap layer and low-k layer corresponds to the desired design thickness). McGahay, in col 4, lines 1-10, discloses that plasma oxidation is performed in plasma chamber on the dielectric layer, and is heated throughout the process (beginning to the end till desired thickness is obtained, i.e., substrate with the dielectric layer is heated throughout the oxide formation process resulting in the forming of the cap layer on the upper portion of the dielectric layer), and is heated to at least 400ºC, i.e., the volatile material present in the layers (dielectric and oxide layers and substrate) are out-gassed via the plasma chamber exhaust system (Precision 5000, by Applied Materials) (claims 1- 5, and 11-15).

The difference between the claims and McGahay is that McGahay does not disclose that the low-k dielectric layer is heat treated for a predetermined period of time after forming the low-k dielectric layer so as to promote out-gassing of volatile materials. McGahay does not disclose during heat treatment the pressure is maintained at less than about 1 Torr (claims 23-24).

Vines, in col 3, lines 43-67, and in col 4, lines 1-7, discloses that following the deposition the dielectric layer, the substrate with the dielectric layer is heat treated at a reduced pressure and elevated temperature (i.e., a vacuum bake), wherein the pressure during the vacuum bake is maintained below 1.0 Torr, and that the reduced pressure

and elevated temperatures causes volatilization of undesired species (i.e., out-gassing of the volatile materials).

Therefore, it would have been obvious to a skilled artisan to have modified McGahay by employing the process of heat treating the substrate with the dielectric layer at the claimed pressure as taught by Vines because Vines, in col 4, lines 50-59, discloses that the anneal process performed on the dielectric layer provides a more reliable film with less tendency to exhibit a charging effect in the finished device.

3. Claims 7-10, and 17-22, are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent No. 6,348,736 (McGahay et al., hereinafter referred to as McGahay) in view of U. S. Patent No. 5,610,105 (Vines et al., hereinafter referred to as Vines) as applied to claims 1-5, 11-15, and 23-24, above and further in view of U. S. Patent Application Publication No. 2002/0090822 (Jiang et al., hereinafter referred to as Jiang).

McGahay in view of Vines is discussed in paragraph no. 2.

McGahay, in col 4, lines 1-1-54, and in col 5, lines 1-62, discloses forming a first resist mask over the sacrificial cap layer (thin oxide layer), and patterning the SSQ layer (low-k dielectric layer) to form a trench opening, forming a second resist mask over the thin oxide layer (even the exposed SSQ layer of the trench is further oxidized to form a thin oxide layer or cap layer) i.e., the patterned SSQ layered substrate is again plasma oxidized prior to second resist mask formation (forming a resist layer and patterning the resist layer to form a second resist mask) and heated (eliminates or out-gasses volatile

material from the SSQ and oxide layers) to form a thin oxide layer in the bottom of the trench; patterning the SSQ layer through the second resist mask to form a via opening, wherein the trench has a greater lateral dimension than the via opening (claims 7-8, 10, 17-18, and 20).

The difference between the claims and McGahay in view of Vines is that McGahay in view of Vines does not disclose that the resist contamination is maintained below a specified level. McGahay in view of Vines does not disclose determining a contamination level of the photoresist or resist residuals prior to forming the first resist mask (claims 9, 19 and 21-22).

Jiang, in [0011], [0012], [0013], [0014], [0015], [0016], [0017], [0018], and [0028], discloses determining the resist poisoning (contamination level in the low-k dielectric layer), and eliminating or reducing the resist poisoning by a corresponding plasma oxidation treatment prior to resist mask formation.

Therefore, it would have been obvious to a skilled artisan to modify McGahay in view of Vines by employing the suggestion of Jiang to determine the resist poisoning amount and reduce the poisoning amount in the low-k dielectric layers prior to further laminations or resist layer formations because McGahay, in col 3, lines 4-16, and in col 4, lines 37-46, discloses that the thin oxide formed on the SSQ dielectric layer is impervious and prevents any contaminants (any attack prevented) from reaching the SSQ dielectric layer, and Jiang, in [0016], [0017], [0018], [0028], and [0030], discloses that plasma oxidation of the low-k dielectric layer, along with heating, reduces resist

poisoning at the via pattern level, and improves the exposure energy, by lowering the required exposure energy needed, for printing the target CD.

(10) Response to Argument

(A) McGahay and Vines do not obviate claims 1-5, 11-15, and 23-24.

I) Appellant argues that there is no motivation or suggestion to combine McGahay and Vines.

McGahay and Vines teach forming a low-k dielectric layer i.e., a silicon containing dielectric layer. Vines is only relied upon to disclose performing a heat treating process after forming the low-k dielectric layer for a predetermined time. McGahay teaches after forming the SSQ i.e., silicon containing dielectric layer, performing a plasma process that includes heating to a high temperature (see col 3, lines 63-67, and in col 4, lines 1-10), see below,

> Referring now to the figures and more particularly to FIG. 1, there is shown an SSQ dielectric layer **14** disposed on an integrated circuit chip **12** rior to dual Damascene processing.
> FIG. **2** shows a thin oxide dielectric layer **16** formed according to the present invention. Preferably, the layer **16** is formed in situ by exposing the SSQ dielectric layer **14** to an oxygen-containing plasma in a suitable processing apparatus (not shown). After formation, the layer **16** preferably is (SiO_2). Any suitable commercially available plasma chamber apparatus can be used, such as a Precision 5000, manufactured by Applied Materials. Preferably, the processing parameters for forming the layer **16** are in the following ranges: 8 to 14 torr pressure, 300 to 1000 W power, 100 to 1000 sccm O2, 350 to 400 C temperature, 1 to 30 seconds process time.

Vines teaches forming a dielectric layer, and heating to a very high temperature, in col 3, lines 43-54, see below,

> Following the PECVD deposition of a dielectric layer, the wafer is heated under a reduced pressure, such as a vacuum or partial vacuum. The vacuum bake acts to free water, hydrogen, and light molecular weight hydrocarbons from the intermetal dielectric film. The vacuum bake uses the volatilizing effects of reduced pressure and elevated temperature to cause the volatilization of undesired species. Generally, the lower the pressure, the lower the temperature can be to achieve a given purity in a given amount of time. Similarly, the time necessary to achieve a given purity can be decreased as the pressure is decreased, and/or the temperature is increased.

Vines as disclosed above, suggests that such heating (after the formation of the dielectric layer) causes volatilization of undesired species, and Vines in col 4, lines 50-59, suggest a good reason i.e., a motivation, see below,

> The vacuum bake followed by the oxidation anneal process allows the PECVD deposited silicon dioxide film to have improved dielectric properties, while minimizing the amount of water, hydrogen, and hydrocarbon present. The relatively low temperature anneal processes herein do not stress the barrier metal structures or cause spiking in the contacts at source/drain junctions. The two-step anneal process also provides a more reliable film, with less tendency to exhibit a charging effect (V_t shift) in the finished device.

i.e., such heating processes (two) not only after forming the dielectric layer (one heating process), but also heating during the exposure of the formed dielectric layer to a plasma oxidation ambient (second heating) i.e., plasma oxidation anneal, results in the formation of a more reliable film with a lesser tendency to exhibit charging effects.

II) Appellant argues that prior art references do not teach all the claim limitations.

McGahay, in col 3, lines 63-67, in col 4, lines 1-67, discloses the formation of a dielectric layer such as a SSQ dielectric layer i.e., a silicon containing dielectric layer, and after formation of the dielectric layer, performing a conversion process i.e., a plasma oxidation process to covert the upper portion of the dielectric layer to an oxide layer i.e., a cap layer (reference 16) is formed on the SSQ dielectric layer (reference 14), and patterning the oxide cap layer and the dielectric layer. McGahay, in col 1, lines 28-30, discloses SSQ as a low-k dielectric materials, see below,

Among such advanced materials having particularly low dielectric constants now in widespread use are some silsesquioxane materials (hereinafter SSQ) which are particularly

McGahay does not teach that prior to the plasma oxidation process that a heat treating is performed on the dielectric layer (low-k) for a predetermined period of time. Vines is depended upon to disclose this limitation i.e., Vines, in col 2, lines 53-56, in col 3, lines 43-54, teaches forming a dielectric layer (a silicon containing dielectric layer), and heating the dielectric layer (i.e., a vacuum bake process) to a very high temperature, prior to the plasma oxidation process i.e., in col 4, lines 20-21, see below,

Following the vacuum bake process, an oxidation anneal is performed. This oxidation anneal acts to oxidize and

Therefore, McGahay in view of Vines teaches all the claim limitations.

III) Appellant argues that the prior art references do not provide a reasonable expectation of success because neither suggests heat treating a low-k dielectric layer prior to forming a cap layer.

McGahay, in col 4, lines 1-10, discloses a plasma oxidation performed on an already formed dielectric layer wherein the oxidation process includes a high temperature heating process which will inherently volatilize any unwanted species present in the dielectric film. However, Vines is relied upon to disclose performing a separate baking process (vacuum bake) prior to the oxidation performed on the dielectric layer. Vines, discloses forming a dielectric layer, and heating the dielectric layer, and then performing an oxidation process, see in col 3, lines 43-49, lines 54-64, and in col 4, lines 20-23, below,

Following the PECVD deposition of a dielectric layer, the wafer is heated under a reduced pressure, such as a vacuum or partial vacuum. The vacuum bake acts to free water, hydrogen, and light molecular weight hydrocarbons from the intermetal dielectric film. The vacuum bake uses the volatilizing effects of reduced pressure and elevated temperature to cause the volatilization of undesired species.

Following the vacuum bake process, an oxidation anneal is performed. This oxidation anneal acts to oxidize and remove any remaining hydrocarbon in the dielectric layer and to improve the silicon oxide quality.

> The vacuum bake step can take place in any appropriate apparatus which can provide both reduced pressure and increased temperature. For example, a horizontal tube furnace or vertical tube furnace can be used. Such furnaces can be single-wafer systems, batch systems, or continuous-batch systems. Horizontal tube furnaces include the Thermco TMX-10000, SVG (Orange, Calif.). Vertical tube furnaces are available, for example, from Tel (Japan), Kokusai (Japan), or SVG (Orange, Calif.). Conveniently, the vacuum bake step can be done in the same apparatus as that used for the subsequent oxidation anneal step.

Therefore, Vines suggests the heat treating process prior to the oxidation process, and there is a reasonable expectation of success, because Vines, cited above, suggests that such heating enables the elimination via volatilization of undesired species in the dielectric film, and that the vacuum bake process prior to the oxidation step can be conveniently performed in the same apparatus as that used for the subsequent oxidation anneal process.

IV) Appellant argues that Vines does not contemplate problems arising form nitrogen or nitrogen compounds diffusing through a low-k dielectric.

The claims (independent claims or dependent claims) do not recite volatile materials as nitrogen or nitrogen compounds; the claims do not recite that nitrogen or nitrogen compounds are out-gassed due to heating. The claims recite that the heat treating promotes out-gassing of volatile materials. See recitation of independent claims 1, and 11, below,

1. (Currently Amended) A method, comprising:

forming a low-k dielectric layer over a substrate;

heat treating said substrate to promote out-gassing of volatile materials for a predetermined period of time after forming the low-k dielectric layer;

converting an upper portion of said low-k dielectric layer into a protective dielectric to form a sacrificial cap layer after heat treating said substrate; and

patterning said sacrificial cap layer and said low-k dielectric layer.

11. (Currently Amended) A method, comprising:

forming a silicon-based low-k dielectric layer over a substrate; and

heat treating said substrate dielectric layer to promote out-gassing of volatile materials for a predetermined period of time after forming the low-k dielectric layer;

forming a silicon dioxide layer as a sacrificial cap layer on said low-k dielectric layer after heat treating said substrate, wherein volatile materials continue to out-gas from said low-k dielectric layer prior to and during the formation of said silicon dioxide layer.

Vines is relied upon to disclose a heat treating process performed prior to the oxidation step, discussed in paragraph III) above, i.e., Vines performs a vacuum bake at a very high temperature such that volatile materials such as hydrogen, hydrocarbons etc., are freed from the dielectric film i.e., out-gassed. The claims recited above, or the

dependent claims do not recite a nitrogen component as the volatile compound or its diffusing effects in a low-k dielectric.

V) Appellant argues that neither McGahay nor Vines recognize the presence of impurities diffusing through the low-k dielectric layer and their resultant effect of resist poisoning.

McGahay as described in paragraphs I) through IV) above, teaches forming a low-k dielectric layer, and performing an oxidation anneal process to form a cap layer (converting the top portion of the dielectric layer to an oxide layer). However, Vines, also described in paragraphs I) through IV) above, is relied upon to disclose the heating performed on the formed dielectric layer prior to performing the oxidation anneal process, and Vines indicates the presence of undesired species i.e., impurities in the dielectric film, and the volatilization of the undesired species during the vacuum bake, and the volatilization of any remaining hydrocarbons (undesired species, materials) during the subsequently performed oxidation anneal process. None of the claims argued above viz., claims 1-5, 11-15, and 23-24, recite an impurity, nor the diffusion of an impurity through a dielectric layer and their resultant effect of resist poisoning. However, resist contamination maintenance levels, and its determination, are addressed in paragraph 3 of the rejection, i.e., McGahay in view of Vines further in view of Jiang. Jiang is relied upon to disclose determination of resist poisoning caused due to the interaction of the resist layer with the underlying low-k dielectric layer i.e., due to the diffusion of materials such as nitrogen in the resists film during subsequent

processings, its determination and elimination of the resist poisoning, see paragraph nos. [01115], through [0014] of Jiang.

VI) Appellant argues that the motivation for combining the references are lacking. This argument has been addressed in argument I) above.

VII) Appellant argues that the impurities or process chemistry described in Vines are simply not an issue and are different than the process employed by the Applicants and as set forth in the claimed subject matter.

The claims recite promoting out-gassing of volatile materials by heat treatment processes performed i) after the formation of a dielectric layer, ii) during the oxidation of the formed dielectric layer (i.e., silicon dioxide layer formation as a cap layer). McGahay teaches performing an oxidation heat treatment process during the formation of a silicon dioxide layer (cap layer) on the already formed low-k dielectric layer (see col 4, lines 1-10). Vines teaches a vacuum bake process on the formed dielectric layer, and an oxidation anneal process on the vacuum baked dielectric layer, wherein both vacuum bake and oxidation anneal processes promote or cause volatilization of undesired species (i.e., volatile materials are out-gassed) (see col 3, lines 43-53, and col 4, lines 20-23). Therefore, the process chemistry taught by Vines is not different from the process limitations as recited in the instant claims.

VIII) Appellant argues that Vines describes a silicon dioxide dielectric layer and that Vines's dielectric layer is a high-k dielectric layer and not a low-k dielectric layer.

McGahay, is relied upon to disclose the low-k dielectric layer. Vines is relied upon to disclose the heating performed on a dielectric layer prior to an oxidation step. McGahay, in col 1, lines 28-30, and in col 3, lines 63-64, discloses that the dielectric layer is an SSQ layer (i.e., silicon based) and that the SSQ is a low dielectric constant material. The claims recite that the low-k dielectric layer comprises a silicon-based dielectric material. See below,

3. (Original) The method of claim 2, wherein said low-k dielectric layer comprises a silicon-based dielectric material.

However, Vines, in col 2, lines 52-61, in col 3, lines 10-54, discloses the formation of a silicon based dielectric layer, wherein prior to the volatilization, the dielectric layer comprises silicon, oxygen, hydrocarbons, hydrogen, and water. Therefore, Vines teaches a dielectric material that is silicon based and is the same dielectric material as that claimed in claim 3.

IX) Appellant argues that there is no recognition in the prior art that nitrogen poisoning is an issue with low-k dielectric layers or that such poisoning may be mitigated by heat treating a low-k dielectric layer.

This argument has been addressed in arguments IV) and V) above. None of the claims of the instant application recite i) nitrogen poisoning in the low-k dielectric layer, and ii) nitrogen poisoning mitigation by heat treating a low-k dielectric layer. Vines is

relied upon to disclose heat treatment to volatilize undesired species (removing undesired species from the dielectric layer to achieve a given purity) i.e., mitigating poisoning (or presence of unwanted species) by heat treating the dielectric layer. See Vines in col 3, lines 43-54, in col 4, lines 20-23.

X) Appellant argues that the combination of McGahay and Vines do not teach all the features of the claimed subject matter because Vines teaches heat treating a silicon dioxide layer as opposed to a low-k dielectric layer.

These arguments have been addressed in arguments II), and VIII) above.

(B) McGahay, Vines and Jiang do not obviate claims 7-10, and 17-22.

I) Appellant argues that Jiang teaches a cap layer formation step without a preceding heat treatment out-gassing step.

Jiang is not relied upon to disclose the cap layer formation or the heat treatment out-gassing step. McGahay in view of Vines is relied upon to disclose the heat treatment out-gassing step, and the cap layer formation step. McGahay, in col 4, lines 1-10, discloses a low-k dielectric layer (SSQ layer) and performing an oxidation heating step, wherein the top layer portion of the dielectric layer is converted to a silicon dioxide layer (cap layer). Vines, teaches performing a vacuum bake on a formed silicon containing dielectric layer so as to cause volatilization of undesired species i.e., out-gassing by heat treatment, followed by a subsequent oxidation anneal step to form

silicon dioxide. Jiang is relied upon to disclose the determination of resist poisoning, and its elimination or reduction.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

dcd

/Daborah Chacko-Davis/

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